What is claimed is:

1. A semiconductor memory device comprising:

a first conductivity type semiconductor substrate; and

a plurality of memory cells constituted of an island-like semiconductor layer which is formed on the semiconductor substrate, and a charge storage layer and a control gate which are formed entirely or partially around a sidewall of the island-like semiconductor layer,

wherein the plurality of memory cells are disposed in series, the island-like semiconductor layer which constitutes the memory cells has cross-sectional areas varying in stages in a horizontal direction of the semiconductor substrate, and an insulating film capable of passing charges is provided at least in a part of a plane of the island-like semiconductor layer horizontal to the semiconductor substrate.

2. The device according to claim 1, wherein the cross-sectional areas of the island-like semiconductor layer are step by step small to the direction of the surface of the semiconductor substrate.

3. The memory device according to claim 1, wherein the cross-sectional areas of the island-like semiconductor layer are step by step large to the direction of the surface of the semiconductor substrate.

4. The device according to claim 1, wherein the cross-sectional area of the island-like semiconductor layer

distant from the semiconductor substrate is equal to that of the island-like semiconductor layer close to the semiconductor substrate.

5. The device according to claim 1, wherein the island-like semiconductor layer involves at least two same sizes of the cross-sectional areas thereof.

6. The device according to claim 1, wherein the plurality of memory cells are electrically insulated from the semiconductor substrate by a second conductivity type impurity diffusion layer formed in the semiconductor substrate or in the island-like semiconductor layer, or by both of said second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

7. The device according to claim 1, wherein at least one of the memory cells is electrically insulated from another memory cell by a second conductivity type impurity diffusion layer formed in the island-like semiconductor layer, or by both said second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed in the second conductivity type impurity diffusion layer.

8. The device according to claim 6, wherein at least one of the memory cells is electrically insulated from another memory cell by a depletion layer formed at a junction of the second conductivity type impurity diffusion layer in the

semiconductor substrate or the island-like semiconductor layer.

9. The device according to claim 7, wherein at least one of the memory cells is electrically insulated from another memory cell by a depletion layer formed at a junction of the second conductivity type impurity diffusion layer in the semiconductor substrate or the island-like semiconductor layer.

10. The device according to claim 1, wherein an impurity diffusion layer is formed on the surface of the semiconductor substrate and serves as common wiring of the memory cells.

11. The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix, wiring for reading out the state of a charge stored in the memory cells is formed in the island-like semiconductor layers, a plurality of the control gates are disposed continuously in one direction so as to form a control gate line, and a plurality of wirings in a direction crossing the control gate line are connected to form a bit line.

12. The device according to claim 1, wherein a gate electrode for selecting the memory cells formed entirely or partially around the sidewall of the island-like semiconductor layer is formed at least on one end of the island-like semiconductor layer and the gate electrode is disposed in series with the memory cells.

13. The device according to claim 11, wherein the island-like semiconductor layer opposed to the gate electrode is electrically insulated from the semiconductor substrate or the memory cells by a second conductivity type impurity diffusion layer formed in the surface of the semiconductor substrate or the island-like semiconductor layer.

14. The device according to claim 11, wherein a second conductivity type impurity diffusion layer, or the second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed therein is/are formed, in self-alignment with the charge storage layer, in a part or the entirety of respective corners of the island-like semiconductor layer having a step shape so that channel layers of memory cells are electrically connected to each other.

15. The device according to claim 11, wherein a second conductivity type impurity diffusion layer, or the second conductivity type impurity diffusion layer and a first conductivity type impurity diffusion layer formed therein is/are formed, in self-alignment with the charge storage layer and the gate electrode, in a part or the entirety of respective corners of the island-like semiconductor layer having a step shape so that a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode are

electrically connected.

16. The device according to claim 1, wherein a plurality of said control gates are disposed close to each other so that channel layers of the memory cells are electrically connected.

17. The device according to claim 11, wherein the control gate and the gate electrode are disposed close to each other so that a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode are electrically connected.

18. The device according to claim 1, further comprising an electrode between the control gates for electrically connecting channel layers of the memory cells.

19. The device according to claim 11, further comprising an electrode between the control gate and the gate electrode for electrically connecting a channel layer of at least one memory cell and another channel layer which is disposed in the island-like semiconductor layer and opposed to the gate electrode.

20. The device according to claim 11, wherein the control gate and a part or the entirety of the gate electrode are made of the same material.

21. The device according to claim 11, wherein the charge storage layer and the gate electrode are made of the same material.

22. The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix and the width of the island-like semiconductor layers in one direction is narrower than the distance between the adjacent island-like semiconductor layers in the same direction.

23. The device according to claim 1, wherein a plurality of said island-like semiconductor layers are arranged in matrix and the distance between the island-like semiconductor layers in one direction is shorter than that between the island-like semiconductor layers in a different direction.

24. A production process of a semiconductor memory device having a plurality of memory cells constituted of a charge storage layer and a control gate which are formed entirely or partially around a sidewall of an island-like semiconductor layer, the process comprising the steps of:

forming at least one preliminary island-like semiconductor layer on or in a semiconductor substrate;

forming a sidewall spacer of a first insulating film on a sidewall of the preliminary island-like semiconductor layer;

etching the semiconductor substrate while using the sidewall spacer as a mask to form the island-like semiconductor layer whose cross-sectional areas in a horizontal direction of the semiconductor substrate vary in stages;

forming a fifteenth insulating film for covering on the

surface of the island-like semiconductor layer and forming sidewall spacers of a sixteenth insulating film on side faces of the island-like semiconductor layer formed in step shape;

selectively removing the fifteenth insulating film using the sidewall spacers as a mask;

forming an insulating film of a single-layer or stacked-layer structure on the island-like semiconductor layer and a first conductive film; and

forming an isolated first conductive films by forming the first conductive film in the form of a sidewall spacer on a sidewall of the island-like semiconductor layer with the intervention of the insulating film.

25. The process according to claim 24, further comprising the step of introducing impurities, in self-alignment with the first conductive film, into a part or the entirety of respective corners of the island-like semiconductor layer whose cross sectional areas in the horizontal direction of the semiconductor substrate vary in stages.

26. The process according to claim 25, further comprising the steps of:

forming an interlayer capacitance film on the isolated first conductive films;

forming a second conductive film on the interlayer capacitance film; and

forming an isolated second conductive films by forming

the second conductive film in the form of a sidewall spacer on sidewalls of the isolated first conductive films with the intervention of the interlayer capacitance film.

27. The process according to claim 25, wherein the impurities introduced into the corners of the island-like semiconductor layer form an impurity diffusion layer by being diffused in the direction horizontal to the surface of the semiconductor substrate so as to be connected to each other.

28. The process according to claim 24, wherein a plurality of said island-like semiconductor layers are formed in matrix in such a manner that the width of the island-like semiconductor layers in one direction become narrower than the distance between the island-like semiconductor layers by removing an oxide film formed by oxidizing the sidewall of the island-like semiconductor layers.

29. The process according to claim 24, wherein a fifth conductive film is formed between the isolated first conductive films.

30. The process according to claim 24, wherein the first conductive film is isolated so that the isolated conductive films are close enough to each other for allowing a channel layer formed in the island-like semiconductor layer under the isolated first conductive films to be electrically connected to an adjacent channel layer.

31. The process according to claim 24, wherein the second

conductive film is isolated so that each of the isolated conductive films are close enough to each charge storage layer for allowing a channel layer formed in the island-like semiconductor layer under the isolated first conductive films to be electrically connected to an adjacent channel layer.

32. The process according to claim 24, further comprising the steps of:

forming an eighteenth insulating film on the first conductive film so as to cover the surface thereof and forming sidewall spacers of the eighteenth insulating film; and

forming the isolated first conductive films in the form of a sidewall spacer using the sidewall spacer of the eighteenth insulating film as a mask.